EECS 2077 Test #3, Fall 2014 Name:_____

#1 ____/25 pts **Allowed materials: 3 pages of 1-sided equation sheets, writing utensil, calculator.**
#2 ____/25 pts **Remember – we use cgs units! Centimeter/gram/second.**
#3 ____/20 pts kT = 0.026 eV (300K) ε_0=8.854x10^{-14} F/cm ε_r(Si)=11.8 ε_r(SiO_2)=4.0
#4 ____/30 pts q= 1.6x10^{-19} C n_i(Si)=1.5x10^{10} / cm^3

Optional Feedback
Rate the length of this test: ***short*** ☐ ***long*** ☐ ***OK*** ☐
Rate the difficulty of this test: ***easy*** ☐ ***hard*** ☐ ***OK*** ☐

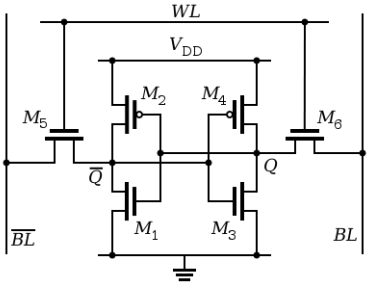
1.) Multiple choice questions, for MOSFETs. Only one answer for each. [5 pts each]

a) The electrical impedance seen at the gate of a MOSFET is very very high for low frequencies because:

[ ] – the input is nearly purely capacitive in nature with almost infinite resistance.
[ ] – the channel under the gate in some cases is depleted of carriers.
[ ] - the gate is made of poly-silicon, not of a metal.
[ ] - of Voodoo magic.

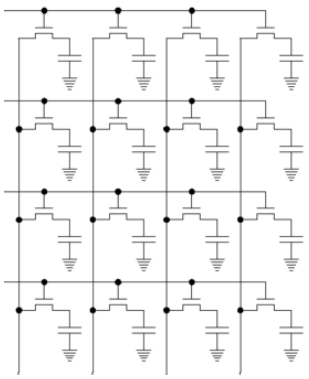
b) Above threshold, externally applied voltage causes inversion carriers in the channel to:
[ ] – increase linearly with voltage
[ ] – increase with the square root of voltage
[ ] - increase exponentially with voltage
[ ] - explode with excitement.

c) If a MOSFET is turned OFF by the gate, the current is small and is limited primarily by:
[ ] – a depleted channel with no carriers and therefore very high resistance.
[ ] – reverse saturation current.
[ ] - diffusion current.
[ ] – severe ennui.



d) The maximum capacitance seen by the gate electrode occurs at:
[ ] - half of the threshold voltage
[ ] - well above threshold voltage
[ ] - right below threshold voltage
[ ] - 2 AM on Friday nights on the way home.

e) Tougher question, which of these would be the <u>least density</u> in terms of bits of storage per cm^2 of chip space? To refresh your memory, diagrams of two of the options are shown at right.
[ ] – DRAM – uses a transistor to charge or discharge a seperate capacitor.
[ ] – SRAM – actively drives bit to a latched state.
[ ] - FLASH – puts an extra floating gate in the gate to store charge.
[ ] – CRISP – what you do to memory when you wire things wrong in electronics lab.

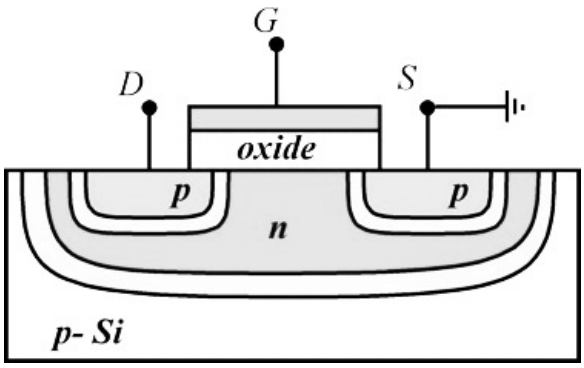


EECS 2077 Test #3, Fall 2014 Name:_____

2) 25 pts. Some variations on questions you have seen before in one way or another…

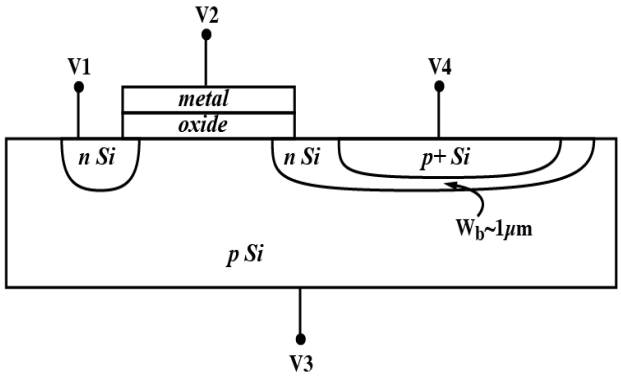
(a) [5 pts.] For the device at right, if I put 0 V on the gate, 0V on the p- Si substrate, and 5 V on the drain, what will the voltage be in the n-type region?

Answer: _____V



(b) [10 pts.] If the device on the left side has a transconductance of $2x10^{-3}$ Siemens or (A/V) and the device on the right has an amplification factor of 200, calculate the change in current at terminal V4 when terminal V2 is changed by 1 V. Assume all other voltages are setup in order to support this amplification.

Answer: _____ A



Some tougher questions, you must get them 100% right to get credit…

(c) [5 pts.] A MOSFET with a threshold voltage of 4 V is biased with 4 V and the depletion width is found to be 200 nm, which of the following must be true (mark all that are correct):

[ ] – the depletion width at 9 V must be 300 nm (square root, like 4V/200 nm).
[ ] – the amount of band bending underneath the oxide surface is equal to 4V.
[ ] – the amount of band bending underneath the oxide surface is less than 4V.
[ ] – the conducting charge in the channel can be predicted exactly by Q=CV (V = 4V, C= oxide capacitance).

(d) [5 pts.] The charge applied to the gate electrode is (mark all of these that are possible):

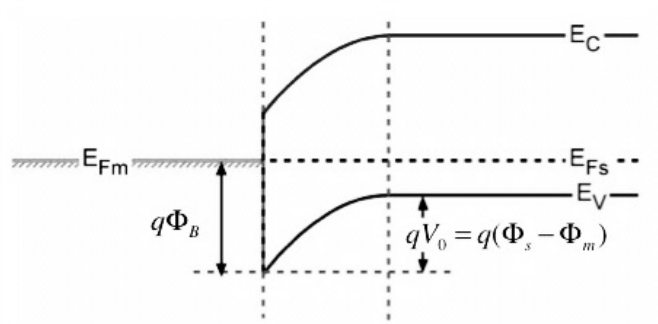
[ ] – equal to the charge created by depletion.
[ ] – equal to the charge created by inversion.
[ ] - equal to the charge created by accumulation.
[ ] - equal to the charge created by depletion and inversion.

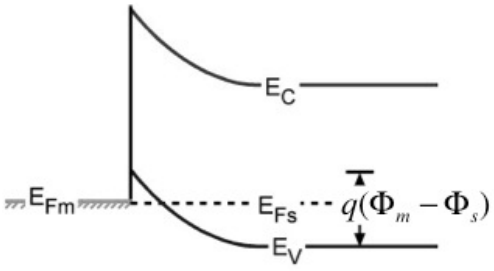
3) 20 pts. Two metal/semiconductor junctions are given below. For both junctions:

a) [8 pts] draw the IV diagram for both positive and negative voltage applied to the junctions, **with respect to voltage applied to the metal** (assume semiconductor is grounded);

b) [6 pts] on each plot, for **positive voltage** label the **carrier type** that dominates the current flow on the semiconductor side of the junction;

c) [6 pts] on each plot, for **negative voltage** label the **carrier type** that dominates the current flow on the semiconductor side of the junction.





EECS 2077 Test #3, Fall 2014 Name:_____

4) [30 pts] Question related to an p-MOS transistor with the following parameters:

The gate electrode 'metal' is n+ poly Silicon.

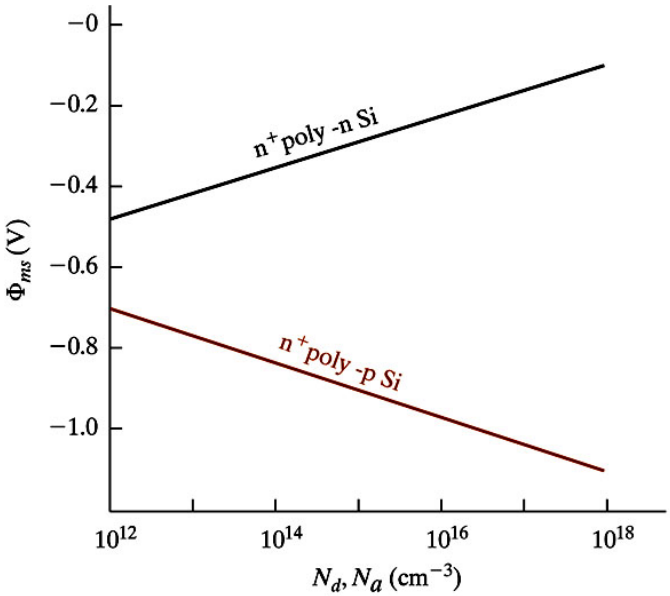
The substrate is doped with Phosphorus to the level of Nd=10^{16}/cm^3.

In the plot shown at right, the curves are labeled as 'gate material – substrate material'.

The gate oxide is has a thickness of 20 nm and a dielectric constant of 4.

There is an interface charge (Qi) of -50 nC/cm^2.

$$V_T = \phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_{D,\max}}{C_i} + 2\phi_f$$



a) provide the value for how much the Fermi level in the substrate has been shifted from the intrinsic Fermi level due to doping (deeper into the substrate, where the bands are flat) [5 pts]:

b) calculate the capacitance per unit area of the gate oxide [5 pts]:

c) provide the value for the maximum depletion charge [5 pts]

d) provide the value for how much threshold voltage is influenced by the fact that the Fermi level of the gate electrode and the Fermi level of the substrate Si, have to shift to match up at equilibrium [5 pts]:

e) calculate the threshold voltage for this device [10 pts]:

EXTRA SPACE